

# Multilevel switching voltage modeling and PWM control strategies for dual two-level converters with open-end winding configuration

Khoa Dang Pham, Nho Van Nguyen\*

## ABSTRACT

Dual Two-level converters with Open-end Winding configuration (DTC-OEWs) feature several advantages over Three-level Neutral Point Clamped converters (3L-NPCs), such as even power loss distribution, no requirement of DC-link voltage balancing, fewer number of switching devices, a great number of redundant switching states. However, Pulse-width modulation strategies (PWMs) applied in Dual Two-level converters with Open-end Winding configuration (DTC-OEWs) involve complex and counter-intuitive time-shifting offset for pulse generation whereas the PWM schemes of the traditional multilevel converters, such as the carrier-based Pulse-width modulation (PWM) strategies are simple. And this renders the Pulse-width modulation (PWM) control in DTC-OEWs complex in comparison to that of the traditional multilevel converters. Therefore, multilevel switching voltage models (ML-SVMs) of the Dual Two-level converters with Open-end Winding configuration (DTC-OEWs) with isolated DC-link sources are proposed in this article, thereby enabling the Dual Two-level converters with Open-end Winding configuration (DTC-OEWs) with isolated DC sources, the three-level Neutral Point Clamped converters (3L-NPCs) and the Three-level Cascaded H-bridge converters (3L-CHBs) to be regarded as a single multilevel-converter entity. Thus, it allows a rich pool of simple and intuitive PWM strategies derived for the 3L-NPCs and the 3L-CHBs to be applied directly to the Dual Two-level converters with Open-end Winding configuration (DTC-OEWs) without any modification. Several Pulse-width modulation (PWM) strategies, which are previously utilized for the Three-level Neutral Point Clamped converters (3L-NPCs) and the Three-level Cascaded H-bridge converters (3L-CHBs), are applied to the Dual Two-level converters with Open-end Winding configuration (DTC-OEWs) by using the multilevel switching voltage models (ML-SVMs). Simulation results of several PWM strategies, including the line voltages, phase currents, and the common-mode voltages from the three-level Neutral-Point Clamped converter (3L-NPC) and the Dual Two-level converter with Open-ends Winding configuration (DTC-OEW) bear a complete resemblance, thereby indicating the correctness of the multilevel switching voltage models.

**Key words:** Cascaded H-bridge Converter, Multilevel Converter Modeling, Neutral Point Clamped Converter, Open-End Winding, Pulse-width Modulation Strategy

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## INTRODUCTION

Multilevel converters have been intensively used in industrial applications such as motor-drive and grid-connected photovoltaic systems due to their superior output quality and lower EMIs in comparison to conventional two-level converters<sup>1</sup>. Several well-known multilevel converter topologies include Three-Level Neutral Point Clamped Converters (3L-NPCs)<sup>2</sup>, Five-Level Cascaded H-bridge Converters (5L-CHB)<sup>3</sup>, and Dual Two-level Converter with Open-End Winding Configuration (DTC-OEWs)<sup>4</sup>. As for 3L-NPCs, Neutral Point (NP) voltage unbalance<sup>5-8</sup> and unequal loss distribution<sup>9</sup> are the main drawbacks. With regard to 5L-CHBs, multiple isolated DC sources are required, thereby increasing the cost and volume of the system. Regarding the Open-End Winding Configurations, they have

gained significant research attention for the last two decades<sup>10-18</sup>. By opening up the neutral point of a motor and connecting the motor to the two converters at both ends, multilevel voltage at the output can be achieved. In the case of DTC-OEWs, three-level voltage can be obtained similar to 3L-NPCs. Under the same number of voltage levels, OEWs possess a number of distinct merits such as no NP unbalance, equal loss distribution, fewer number of switching devices, a larger number of redundant switching states, and a smaller number of isolated DC sources in comparison to NPCs and CHBs.

With respect to DC sources, OEWs can be categorized into two forms, i.e., OEWs with isolated DC sources and OEWs with a common DC source. OEWs with isolated DC sources is typically used at high power<sup>19</sup> while OEWs with a common DC source utilizes a single DC source for economical purposes<sup>20</sup>. Neverthe-

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less, the focus of this paper is on the DTC-OEW with isolated DC sources. As for the DTC-OEW with a common DC source, it will be discussed in detail in a separate paper.

Unlike 3L-NPC and CHB which employs Carrier-based pulse-width modulation (CB-PWM) strategies, PWM schemes applied to OEWs are complex and counter-intuitive, involving the time-offset shifting to attain certain modulation modes such as Maximum Discontinuous PWM (Max-DPWM), Min Discontinuous PWM (Min-DPWM), Centered SVPWM (CSVPWM)<sup>21</sup>. To address this issue, ML-SVMs of DTC-OEWs with isolated DC sources are proposed in this article. The proposed ML-SVMs for DTC-OEWs possess two distinct advantages. First, they enable the DTC-OEWs to be viewed as a single multilevel converter entity. In other words, DTC-OEWs, 3L-NPCs, and 3L-CHBs can be regarded as one single multilevel converter due to having the same ML-SVMs. The ML-SVMs of the NPC and CHB are presented in<sup>22-24</sup>, allowing them to be viewed as a single multilevel converter entity. Hence, a comparison of the ML-SVMs of DTC-OEWs, 3L-NPCs, and 3L-CHB are shown in this article. Second, the proposed ML-SVMs allow all simple and intuitive PWM strategies, specifically CB-PWM with offset addition previously applied for NPC and CHB, to be directly utilized for DTC-OEWs without modification, thus avoiding the complex time-offset-shifting PWM schemes in DTC-OEWs.

The main contributions of the article are as follows: Firstly, ML-SVMs of the DTC-OEW with isolated DC sources are proposed, being equivalent to those of the 3L-NPC and the 3L-CHB.

Secondly, the proposed ML-SVMs of the DTC-OEW with isolated DC sources enables the direct application of the PWM strategies, which have been previously applied to the 3L-NPC and the 3L-CHB, thus taking advantage of the simplicity of implementation of the CB-PWM strategies while avoiding the complex and counter-intuitive time-offset-shifting PWM schemes in the DTC-OEWs.

Thirdly, with the aid of the proposed ML-SVMs, three PWM strategies, i.e., RCMV1, POD-SPWM, and IPD-SPWM, which have been previously applied to the 3L-NPC and the 3L-CHB, are implemented in detail for the DTC-OEW with isolated DC sources, thus emphasizing the contribution of the ML-SVMs of the DTC-OEW.

Finally, the equivalence between the ML-SVMs of the DTC and the 3L-NPC is confirmed by the simulation results, including the waveforms of the phase voltage,

the phase current, and the CMV along with their frequency spectra and THD analyses.

The article is organized as follows:

Section (2) presents the Multilevel Switching Voltage Models of Multilevel Converters.

Specifically, the sub-section (2.1) briefly presents ML-SVMs of the 3L-NPC and the 3L-CHB, serving as a foundation for the sub-section (2.2).

The sub-section (2.2) presents the ML-SVM of the DTC-OEW with isolated DC sources. In addition, A summary of ML-SVMs of the DTC-OEW with isolated DC sources, the 3L-NPC, and the 3L-CHB is also made, indicating the exact same ML-SVMs and mathematical expressions for all three mentioned topologies.

The sub-section (2.3) demonstrates the implementation of three PWM schemes previously applied to 3L-NPCs and 3L-CHBs, specifically Reduced-CMV PWM1 (RCMV1)<sup>24</sup>, Phase Opposition Disposition Sinusoidal PWM (POD-SPWM)<sup>24</sup>, and In-Phase Disposition Sinusoidal PWM (IPD-SPWM)<sup>24</sup> with the help of ML-SVMs.

Section (3) shows the simulation results including the waveforms of the phase voltage, the phase current and the CMV of the DTC-OEW with isolated DC sources and the 3L-NPC, confirming both ML-SVMs are equivalent. THD analyses of the phase voltage and phase current along with their frequency spectra are also demonstrated for both the DTC-OEW with isolated DC sources and the 3L-NPC.

Section (4) concludes the article with some key remarks.

## MULTI-LEVEL SWITCHING VOLTAGE MODELS (ML-SVMs) OF MULTILEVEL CONVERTERS AND PWM IMPLEMENTATION – METHOD SECTION

### ML-SVMs of 3L-NPCs and 3L-CHBs

This section briefly reviews the ML-SVMs of the 3L-NPC and the 3L-CHB. Instantaneous and average ML-SVMs as well as corresponding mathematical expressions are shown, serving as a foundation for the subsequent sections.

Under the condition of balanced DC-link voltages, which can be satisfied with the isolated transformer, the instantaneous pole voltage of the phase leg x,  $x \in \{A, B, C\}$  of the 3L-NPC and 3L-CHB can be expressed as:

$$V_{x0} = (S_{1x} + S_{2x}) \times V_{DC} - V_{DC} \quad (1)$$

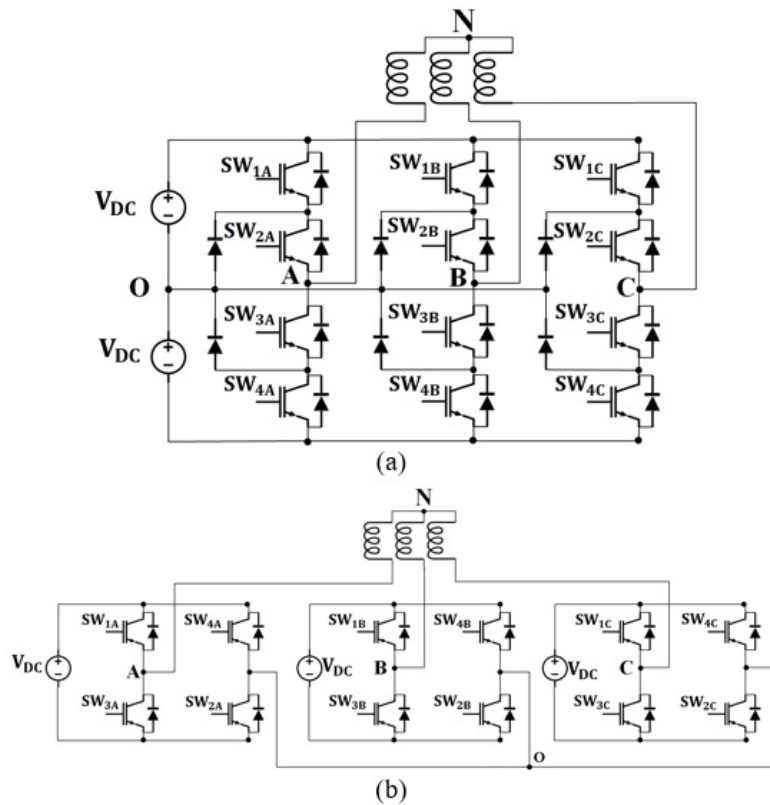


Figure 1: Topologies of (a) the 3L-NPC and (b) the 3L-CHB.

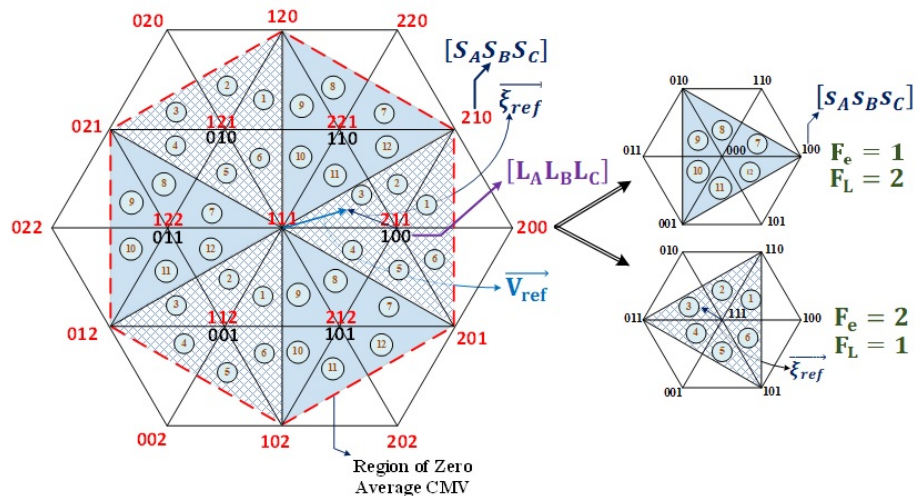


Figure 2: A three-level space vector diagram constituting two types of two-level switching diagrams, i.e., ( $F_e = 1$ ,  $F_L = 2$ ) and ( $F_e = 2$ ,  $F_L = 1$ ).

where:  $V_{xO}$  is the instantaneous pole voltage of phase leg  $x$ ,  $x \in \{A, B, C\}$ , as shown in Figure 1.  $S_{1x}$  and  $S_{2x}$  are the switching states of the switches  $SW_{1x}$  and  $SW_{2x}$  respectively, taking a value of 0 or 1. For instance,  $S_{1x} = 0$  means  $SW_{1x}$  is OFF and vice versa.  $S_{2x} = 0$  means  $SW_{2x}$  is OFF and vice versa.

It is also worth noting that there is a restriction for  $(S_{1A}, S_{2A})$ ,  $(S_{1B}, S_{2B})$ , and  $(S_{1C}, S_{2C})$  in the 3L-NPC, specifically  $S_{1A} \leq S_{2A}$ ,  $S_{1B} \leq S_{2B}$ , and  $S_{1C} \leq S_{2C}$ . However, there is no such restriction for the 3L-CHB. This characteristic is known as phase-leg redundancy<sup>23</sup>.

Let  $S_A$ ,  $S_B$ , and  $S_C$  denote  $S_{1A} + S_{2A}$ ,  $S_{1B} + S_{2B}$ , and  $S_{1C} + S_{2C}$  respectively. Eq. (1) can be expressed as:

$$V_{AO} = S_A \times V_{DC} - V_{DC} \quad (2)$$

$$V_{BO} = S_B \times V_{DC} - V_{DC} \quad (3)$$

$$V_{CO} = S_C \times V_{DC} - V_{DC} \quad (4)$$

where:  $S_A$ ,  $S_B$ , and  $S_C$  are the normalized three-level switching voltages (normalized with  $V_{DC}$ ) of phase A, B, and C respectively, assuming a value of 0, 1, or 2.

The normalized instantaneous three-level switching voltages  $S_A$ ,  $S_B$ , and  $S_C$  can be decomposed into 2 components as follows:

$$S_A = s_A + L_A \quad (5)$$

$$S_B = s_B + L_B \quad (6)$$

$$S_C = s_C + L_C \quad (7)$$

where:  $s_A$ ,  $s_B$ , and  $s_C$  are the normalized two-level switching voltages of phase A, B, and C respectively, taking a value of 0 or 1.  $L_A$ ,  $L_B$ , and  $L_C$  are the base voltages of phase A, B, and C respectively, also assuming a value of 0 or 1.

The normalized three-level switching voltages  $[s_A, s_B, s_C]$ , the normalized two-level switching voltages  $[s_A, s_B, s_C]$ , and the base voltages  $[L_A, L_B, L_C]$  are illustrated in Figure 2.

From (2) - (7), the instantaneous CMV can be derived as follows:

$$V_{CMV} = \frac{(S_A + S_B + S_C - 3) V_{DC}}{3} \quad (8)$$

The normalized average three-level switching voltages of phase A, B, and C can be written as:

$$\begin{aligned} v'_{Aref} &= v_{Aref} + v_{off} \\ &= \frac{2m}{\sqrt{3}} \times \cos(\omega t) + v_{off} \end{aligned} \quad (9)$$

$$\begin{aligned} v'_{Bref} &= v_{Bref} + v_{off} \\ &= \frac{2m}{\sqrt{3}} \times \cos\left(\omega t - \frac{2\pi}{3}\right) + v_{off} \end{aligned} \quad (10)$$

$$\begin{aligned} v'_{Cref} &= v_{Cref} + v_{off} \\ &= \frac{2m}{\sqrt{3}} \times \cos\left(\omega t - \frac{4\pi}{3}\right) + v_{off} \end{aligned} \quad (11)$$

$$m = \frac{1}{\sqrt{3}} V_{DC} \quad (12)$$

where:  $v_{Aref}$ ,  $v_{Bref}$ , and  $v_{Cref}$  are the normalized reference load voltages.  $m$  is the modulation index, the range of which depends on the value of  $v_{off}$ .  $v_{1m}$  is the fundamental magnitude of the phase voltage.  $v_{off}$  is the normalized offset voltage ranging from  $v_{offmin}$  to  $v_{offmax}$  i.e.,

$$v_{offmin} \leq v_{off} \leq v_{offmax} \quad (13)$$

$$v_{offmax} = 2 - \text{Max}\{v_{Aref}, v_{Bref}, v_{Cref}\} \quad (14)$$

$$v_{offmin} = -\text{Min}\{v_{Aref}, v_{Bref}, v_{Cref}\} \quad (15)$$

The average CMV can be written as:

$$\begin{aligned} v_{CMV} &= \frac{(v'_{Aref} + v'_{Bref} + v'_{Cref} - 3) v_{DC}}{3} \\ &= \frac{(3v_{off} - 3) v_{DC}}{3} \end{aligned} \quad (16)$$

Different values of  $v_{off}$  can lead to different operating modes such as Maximum Discontinuous PWM (Max-DPWM) with  $v_{off} = v_{offmax}$ , Minimum Discontinuous PWM (Min-DPWM) with  $v_{off} = v_{offmin}$ , and Reduced CMV PWM (RCMV) with  $v_{off} = 1$ .

The normalized average three-level switching voltages of three phases A, B, and C can also be expressed as:

$$v'_{Aref} = \xi_A + L_A \quad (17)$$

$$v'_{Bref} = \xi_B + L_B \quad (18)$$

$$v'_{Cref} = \xi_C + L_C \quad (19)$$

$$L_A = \text{floor}\left(v'_{Aref}\right) \quad (20)$$

$$L_B = \text{floor}\left(v'_{Bref}\right) \quad (21)$$

$$L_C = \text{floor}\left(v'_{Cref}\right) \quad (22)$$

where:  $\xi_A$ ,  $\xi_B$ , and  $\xi_C$  are the normalized average two-level switching voltages with values ranging from 0 to 1.  $L_A$ ,  $L_B$ , and  $L_C$  are the base voltages of phase A, B and C respectively, also assuming a value of 0 or 1, as mentioned previously.

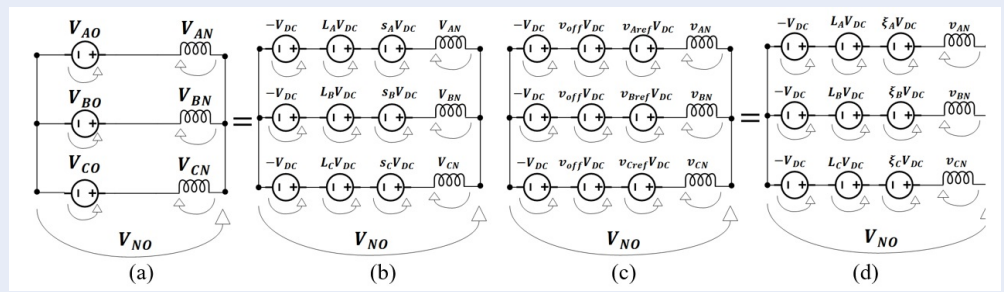
The total base voltage  $F_L$  can be defined as:

$$F_L = L_A + L_B + L_C \quad (23)$$

The total two-level switching voltage  $F_e$  can be defined as:

$$F_e = \xi_A + \xi_B + \xi_C \quad (24)$$

The instantaneous and average ML-SVMs of the 3L-NPC and the 3L-CHB are demonstrated in Figure 3.



**Figure 3:** (a) Instantaneous ML-SVMs of the 3L-NPC and the 3L-CHB comprising the instantaneous pole voltages (b) Instantaneous ML-SVMs of the 3L-NPC and the 3L-CHB comprising the base voltages and instantaneous two-level switching voltages (c) Average ML-SVMs of the 3L-NPC and the 3L-CHB comprising the average reference load voltages and average offset voltages (d) Average ML-SVMs of the 3L-NPC and the 3L-CHB comprising the base voltages and average two-level switching voltages.

### Proposed ML-SVMs of DTC-OEWs with isolated DC sources

The primary goal of this section is to bring the models of the DTC-OEWs back to the ML-SVMs of the 3L-NPC and the 3L-CHB, allowing the DTC-OEWs, the 3L-NPC and the 3L-CHB to be viewed as a single multilevel-converter entity.

For the purpose of comparison among DTC-OEWs, 3L-NPCs, and 3L-CHBs, a table which lists various aspects of the converters including the number of semiconductor devices used, voltage stress on the switches, modulation range, imbalance on the DC-link capacitor, and common-mode voltage magnitudes is shown in Table 1.

The individual instantaneous pole voltages of Inverter 1 and Inverter 2 can be expressed as:

$$V_{x10} = S_{1x} \times V_{DC}, x \in \{A, B, C\} \quad (25)$$

$$V_{x20'} = (1 - S_{2x}) \times V_{DC}, x \in \{A, B, C\} \quad (26)$$

where:  $V_{x10}$  and  $V_{x20'}$  are the pole voltage of phase leg  $x$ ,  $x \in \{A, B, C\}$  of Inverter 1 and 2 respectively, as shown in Figure 4.  $S_{1x}$  and  $S_{2x}$  are the switching states of the switches  $SW_{1x}$  and  $SW_{2x}$  respectively, taking a value of 0 or 1. For instance,  $S_{1x} = 0$  means  $SW_{1x}$  is OFF and vice versa.  $S_{2x} = 0$  means  $SW_{2x}$  is OFF and vice versa.

From (25) and (26), the difference of the individual pole voltages is called generic pole voltage of the DTC-OEW and is expressed for the three phases  $A_1A_2$ ,  $B_1B_2$ , and  $C_1C_2$  as follows:

$$\begin{aligned} V_{A10} - V_{A20'} &= V_{A1A2} + V_{O'O} \\ &= (S_{1A} + S_{2A}) V_{DC} - V_{DC} \end{aligned} \quad (27)$$

$$\begin{aligned} V_{B10} - V_{B20'} &= V_{B1B2} + V_{O'O} \\ &= (S_{1B} + S_{2B}) V_{DC} - V_{DC} \end{aligned} \quad (28)$$

$$\begin{aligned} V_{C10} - V_{C20'} &= V_{C1C2} + V_{O'O} \\ &= (S_{1C} + S_{2C}) V_{DC} - V_{DC} \end{aligned} \quad (29)$$

where:  $V_{A1A2}$ ,  $V_{B1B2}$ ,  $V_{C1C2}$  are the instantaneous phase voltages of three phases  $A_1A_2$ ,  $B_1B_2$ , and  $C_1C_2$  respectively.  $V_{O'O'}$  is the instantaneous common-mode voltage (CMV), as illustrated in Figure 4 and Figure 5.

Similar to the 3L-CHB, there is no restriction for  $(S_{1A}, S_{2A})$ ,  $(S_{1B}, S_{2B})$ , and  $(S_{1C}, S_{2C})$  in the DTC-OEW with isolated DC sources. Hence, the phase-leg redundancy also exists in the DTC-OEW with isolated DC sources.

Figure 5(a) demonstrates a simplified view of the DTC-OEW with isolated DC sources, consisting of two two-level Voltage Source Inverters (VSIs). From which, the instantaneous SVM of the DTC-OEW, comprising individual instantaneous pole voltages of two VSIs, can be then derived, as demonstrated in Figure 5(b).

Using Kirchoff voltage's law and Eq. (27)-(29), the circuit manipulation of the instantaneous SVM of the DTC-OEW in Figure 5(b) leads to the instantaneous ML-SVM in Figure 5(c) for the case of the isolated DC sources. This ML-SVM of the DTC-OEW is equivalent to those of the 3L-NPC and the 3L-CHB, as shown in Figure 3(a).

The generic instantaneous pole voltages of the DTC-OEW with isolated DC sources contain the instantaneous phase voltages  $V_{A1A2}$ ,  $V_{B1B2}$ ,  $V_{C1C2}$ , and the instantaneous CMV  $V_{O'O'}$ . Similarly, the instantaneous pole voltages of the 3L-NPC and the 3L-CHB also contain the instantaneous phase voltages  $V_{AN}$ ,  $V_{BN}$ ,  $V_{CN}$ , and the instantaneous CMV  $V_{O'O'}$ .

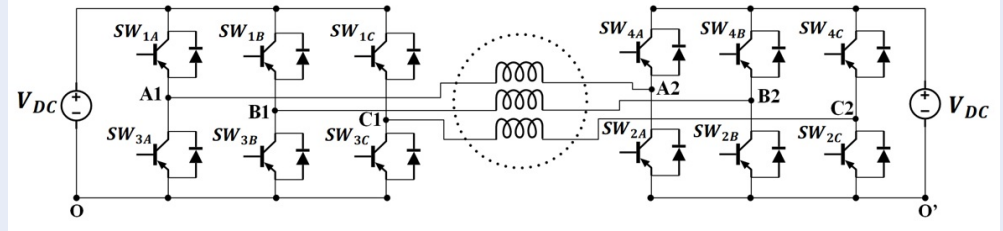


Figure 4: A DTC-OEW with isolated DC sources

Table 1: Comparison Table under Various Aspects for 3L-NPCs, DTC-OEWs, and 3L-CHBs

Comparison Aspects	3L-NPCs	DTC-OEWs	3L-CHBs
Number of Semiconductor Devices	IGBTs with free-wheeling diodes	12	12
	Diodes	6	0
Voltage Stress on the Switches	$V_{DC}$	$V_{DC}$	$V_{DC}$
Modulation Range in RCMV1	$0 \leq M \leq \frac{\sqrt{3}}{2}$	$0 \leq M \leq \frac{\sqrt{3}}{2}$	$0 \leq M \leq \frac{\sqrt{3}}{2}$
Imbalance on DC-link capacitor	Yes	No	No
Common-mode voltage magnitudes in RCMV1	$\pm V_{DC}/3$	$\pm V_{DC}/3$	$\pm V_{DC}/3$

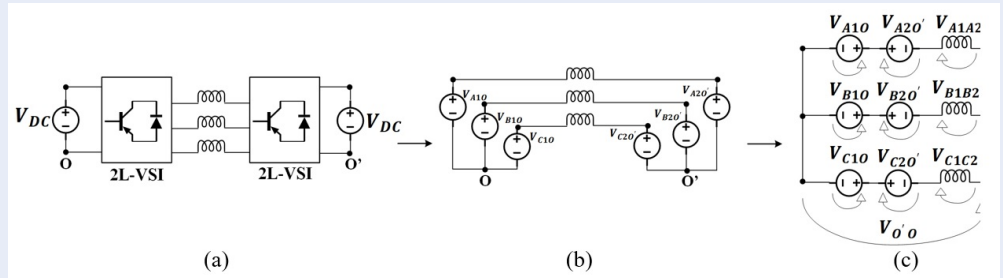


Figure 5: A DTC-OEW with isolated DC sources under (a) A simplified view (b) An Instantaneous SVM comprising individual instantaneous pole voltages and (c) Instantaneous ML-SVM.

Let  $S_A$ ,  $S_B$ , and  $S_C$  denote  $(S_{1A} + S_{2A})$ ,  $(S_{1B} + S_{2B})$ , and  $(S_{1C} + S_{2C})$  respectively. Eq. (27)-(29) can be expressed as:

$$\begin{aligned} V_{A10} - V_{A20'} &= V_{A1A2} + V_{O'O} \\ &= S_A V_{DC} - V_{DC} \end{aligned} \quad (30)$$

$$\begin{aligned} V_{B10} - V_{B20'} &= V_{B1B2} + V_{O'O} \\ &= S_B V_{DC} - V_{DC} \end{aligned} \quad (31)$$

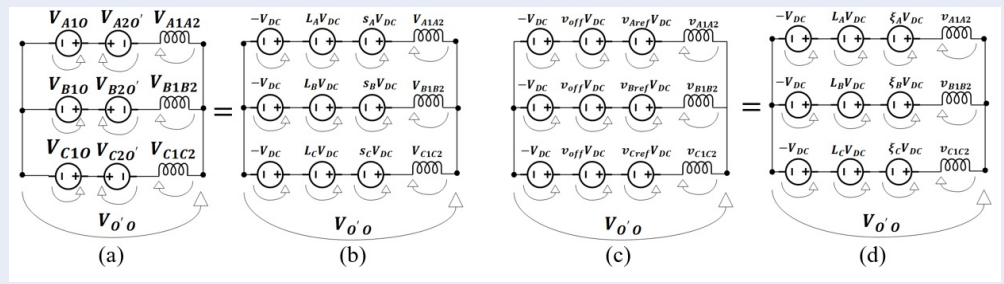
$$\begin{aligned} V_{C10} - V_{C20'} &= V_{C1C2} + V_{O'O} \\ &= S_C V_{DC} - V_{DC} \end{aligned} \quad (32)$$

where:  $S_A$ ,  $S_B$ , and  $S_C$  are the normalized three-level switching voltages (normalized with  $V_{DC}$ ) of three phases  $A_1A_2$ ,  $B_1B_2$ , and  $C_1C_2$  respectively, assuming a value of 0, 1, or 2.

The generic pole voltages of the DTC-OEW with isolated DC sources in Eq. (30)-(32) are exactly of the same forms as those of the 3L-NPC and the 3L-CHB in Eq. (2)-(4). Hence, the instantaneous and average ML-SVMs of the 3L-NPC and the 3L-CHB can also be applied to the DTC-OEW with isolated DC sources, as shown in Figure 6.

Since the DTC-OEW with isolated DC sources has the same ML-SVMs as those of the 3L-NPC and the 3L-CHB, Eq. (5)-(24) are also the same for the DTC-OEW with isolated DC sources. Hence, they are not repeated here for brevity.

To better summarize what has been discussed, the switching voltage models' mathematical expressions



**Figure 6:** (a) Instantaneous ML-SVMs of the DTC-OEW with isolated DC sources comprising the instantaneous pole voltages (b) Instantaneous ML-SVMs of the DTC-OEW with isolated DC sources comprising the base voltages and instantaneous two-level switching voltages (c) Average ML-SVMs of the DTC-OEW with isolated DC sources comprising the average reference load voltages and average offset voltages. (d) Average ML-SVMs of the DTC-OEW with isolated DC sources comprising the base voltages and average two-level switching voltages.

**Table 2: ML-SVMs' mathematical expressions of the DTC-OEWs, the 3L-NPC, and the 3L-CHB**

Category	DTC-OEWs Isolated DC sources	3L-NPC & 3L-CHB
Generic Instantaneous Pole Voltages	$V_{A10} - V_{A20}' = V_{A1A2} + V_{O'O} = S_A V_{DC} - V_{DC}$ (27)	$V_{AO} = V_{AN} + V_{NO} = S_A V_{DC} - V_{DC}$ (2)
	$V_{B10} - V_{B20}' = V_{B1B2} + V_{O'O} = S_B V_{DC} - V_{DC}$ (28)	$V_{BO} = V_{BN} + V_{NO} = S_B V_{DC} - V_{DC}$ (3)
	$V_{C10} - V_{C20}' = V_{C1C2} + V_{O'O} = S_C V_{DC} - V_{DC}$ (29)	$V_{CO} = V_{CN} + V_{NO} = S_C V_{DC} - V_{DC}$ (4)
Normalized Instantaneous Three-level Switching Voltages	$S_A = S_{1A} + S_{2A} = s_A + L_A$ (5)	
	$S_B = S_{1B} + S_{2B} = s_B + L_B$ (6)	
	$S_C = S_{1C} + S_{2C} = s_C + L_C$ (7)	
Normalized Average Reference Voltages	$v_{Aref}' = v_{Aref} + v_{off} = \frac{2m}{\sqrt{3}} \cos(\omega t) + v_{off} = \xi_A + L_A$ (9)	
	$v_{Bref}' = v_{Bref} + v_{off} = \frac{2m}{\sqrt{3}} \cos(\omega t - \frac{2\pi}{3}) + v_{off} = \xi_B + L_B$ (10)	
	$v_{Cref}' = v_{Cref} + v_{off} = \frac{2m}{\sqrt{3}} \cos(\omega t - \frac{4\pi}{3}) + v_{off} = \xi_C + L_C$ (11)	

of the DTC-OEWs, the 3L-NPC, and the 3L-CHB are tabulated in Table 2.

### Implementation of PWM Strategies with ML-SVMs of DTC-OEWs

With the aid of the ML-SVMs of the DTC-OEWs, the implementation of three PWM strategies, i.e., In-Phase Disposition Sinusoidal PWM (IPD-SPWM)<sup>24</sup>, Phase Opposition Disposition Sinusoidal PWM (POD-SPWM)<sup>24</sup>, and Reduced CMV PWM1 (RCMV1)<sup>24</sup>, which are previously applied for a 3L-NPC, are utilized for the DTC-OEW with isolated DC sources, as shown in Figure 7. The detailed procedure of implementation is described as follows.

#### IPD-SPWM and POD-SPWM

IPD-SPWM makes use of three nearest vectors to synthesize the reference vector, thus leading to superior output harmonic distortion at the expense of higher CMV magnitude when compared to POD-SPWM<sup>24</sup>. POD-SPWM, on the other hand, achieves lower CMV magnitude at the expense of inferior output harmonic distortion when compared to IPD-SPWM<sup>24</sup>.

IPD-SPWM and POD-SPWM are implemented in a carrier-based manner, as shown in Figure 7(a) and (b), which involves the comparison of the three normalized average three-level switching voltages ( $v_{Aref}'$ ,  $v_{Bref}'$ ,  $v_{Cref}'$ ) with the two triangular signals ranging from 0 to 2. Specifically, the first triangular signal ( $v_{carrier1}$ ) ranges from 0 to 1 while the second one ( $v_{carrier2}$ ) varies from 1 to 2. The results of such comparison give rise to the three normalized instantaneous three-level switching voltages ( $S_A$ ,  $S_B$ ,  $S_C$ ). Based on which, the firing signals ( $S_{1A}$ ,  $S_{2A}$ ), ( $S_{1B}$ ,  $S_{2B}$ ), and ( $S_{1C}$ ,  $S_{2C}$ ) can be derived. To clearly demonstrate the previously described algorithm, the flowchart has been given in Figure 8.

As for  $S_x == 1$ ,  $x \in \{A, B, C\}$ , the phase-leg redundancy exists for the DTC-OEW with isolated DC sources. Specifically, either  $S_{x1} = 1$ ;  $S_{x2} = 0$  or  $S_{x1} = 0$ ;  $S_{x2} = 1$  can be used. In this article, they are utilized to evenly distribute the power loss between Inverter 1 and 2 of the DTC-OEW in a similar fashion as presented in<sup>22</sup> for the CHB. It is noted that Figure 7(a) and (b) only show the case of  $S_{x1} = 0$ ;  $S_{x2} = 1$  for brevity.

### RCMV1

RCMV1 is proposed in<sup>24</sup> for the 3L-NPC with the aim of reducing the CMV and improving the output harmonic distortion in comparison to POD-SPWM. Specifically, RCMV1 maintains zero average CMV and reduced CMV magnitudes while producing better output harmonic distortion in comparison to POD-SPWM<sup>24</sup>. With the proposed ML-SVMs of the DTC-OEW with isolated DC sources, RCMV1 can be directly applied to the DTC-OEW with no modification, thus demonstrating the contribution of the ML-SVMs of the DTC-OEW.

The implementation of the switching sequence under RCMV1 is also illustrated in Figure 7(c) as the reference voltage vector  $\overline{V_{ref}}$  is in the location, as shown in Figure 2. The switching sequences under RCMV1 for other locations are detailed in<sup>24</sup>. Hence, they are not repeated here. Nevertheless, the procedure of implementation is briefly described here.

Each specific location can be uniquely identified with the relation of the normalized average two-level switching voltages ( $\xi_A, \xi_B, \xi_C$ ) and the base voltages ( $L_A, L_B, L_C$ ), as calculated in Eq. (17) - (22). For example, the location of the reference voltage vector in Figure 2 can be identified as  $\xi_B \geq \xi_C \geq \xi_A$  and  $L_A = 1, L_B = 0, L_C = 0$ . For each location, under RCMV1, a specific switching sequence is used to synthesize the reference vector. Figure 7(c) illustrates the switching sequence used for the synthesis of  $\overline{V_{ref}}$  in Figure 2 under RCMV1. The normalized instantaneous three-level switching voltages ( $S_A, S_B, S_C$ ) can be derived as shown in Figure 7(c). Based on which, the firing signals ( $S_{1A}, S_{2A}$ ), ( $S_{1B}, S_{2B}$ ), and ( $S_{1C}, S_{2C}$ ) can be obtained following the previous pseudo-code presented for IPD-SPWM and POD-SPWM. Moreover, the phase-leg redundancy is also utilized to evenly distribute the power loss between Inverter 1 and 2.

## SIMULATION RESULTS AND DISCUSSION

Three PWM strategies, particularly IPD-SPWM, POD-SPWM, and RCMV1, are implemented for the DTC-OEWs with isolated DC sources under MATLAB/Simulink. Phase-voltage waveforms of the DTC-OEWs and the 3L-NPC as well as their total harmonic distortion analyses are shown in Figure 9-Figures 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 20, 21 and 22. For the DTC-OEW with isolated DC sources, the linear modulation range can be extended to  $m = 1$ . However, for simplicity, the linear modulation range (0-0.866) is shown for the case of isolated DC sources. Simulation parameters are listed in Table 3.

**Table 3: Simulation Parameters**

Parameters	Values
Rated Apparent Power	100KVA
DC-link Voltage	$V_{DC} = 200V$
DC-link Capacitor	$C = 4700\mu F$
Fundamental Frequency	$f_m = 50Hz$
Carrier Frequency	$f_c = 5KHz$
Three-phase RL Load	R = 5, L = 7.5mH
Power Factor	0.9
Offset Voltage	$v_{off} = 1$

As for the THD analyses in this section, the THD of output voltage and current can be defined respectively as follows<sup>24</sup>:

$$THD_V = \frac{1}{V_m} \sqrt{\sum_{n=2}^{\infty} V_n^2} \quad (33)$$

$$THD_I = \frac{1}{I_m} \sqrt{\sum_{n=2}^{\infty} I_n^2} \quad (34)$$

where  $V_m$  and  $V_n$  are the fundamental magnitude of phase voltage output and the magnitude of phase voltage output corresponding to harmonic n, respectively.  $I_m$  and  $I_n$  are the fundamental magnitude of phase current output and the magnitude of phase current output corresponding to harmonic n, respectively. The equivalence of the ML-SVMs between the DTC-OEW with isolated sources and the 3L-NPC is confirmed by the waveforms of phase voltage, phase current, and CMV along with their frequency spectra and THD analyses.

The phase voltage waveforms of the DTC-OEW with isolated DC sources are shown in Figure 9 and compared with those of the 3L-NPC in Figure 10 for  $m = 0.8$  under RCMV1, POD-SPWM, and IPD-SPWM. As can be seen from these figures, these waveforms are completely identical, indicating the equivalence of the ML-SVMs. And the similarity in the phase voltage waveforms is substantiated by their frequency spectra for  $m = 0.8$  under three PWM schemes, as shown in Figure 11 and Figure 12 for the DTC-OEW and the 3L-NPC respectively. As can be observed in Figure 11 and Figure 12, the harmonic distribution of phase voltage under three PWM schemes in the DTC-OEW bears a resemblance to that in the 3L-NPC. Specifically, under RCMV1 and  $m = 0.8$ , the carrier-frequency component is around 18.4% in the DTC-OEW as opposed to 18.5% in the 3L-NPC, as illustrated in Figure 11(a) and Figure 12(a) respectively. Moreover, the resemblance in the phase voltage waveforms in both topologies is further confirmed by the

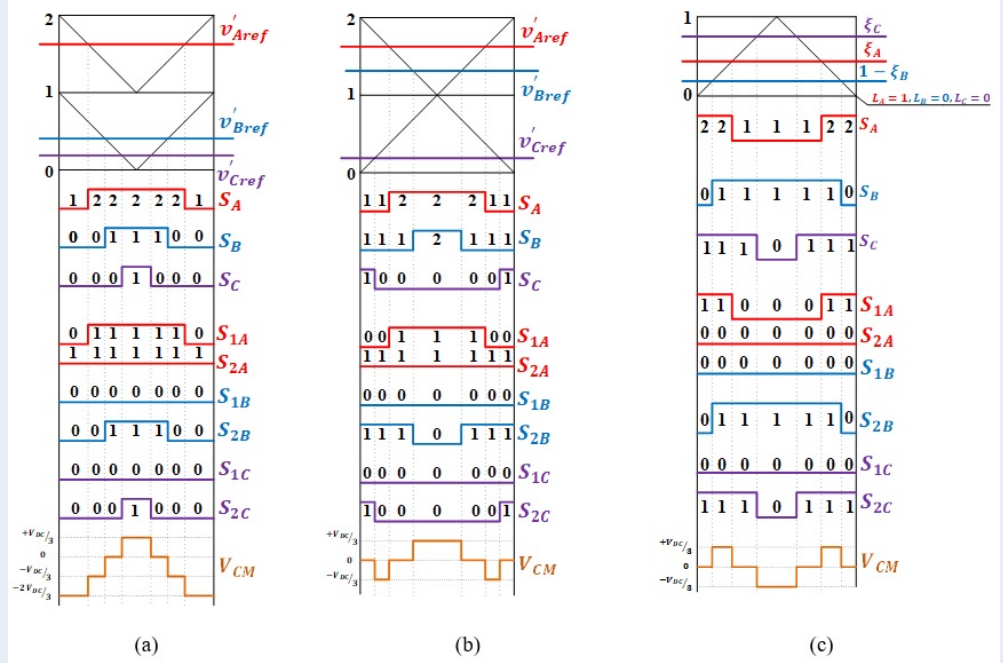


Figure 7: Implementation of the per-carrier switching sequence for the DTC-OEWs under (a) IPD-SPWM (b) POD-SPWM and (c) RCMV1.

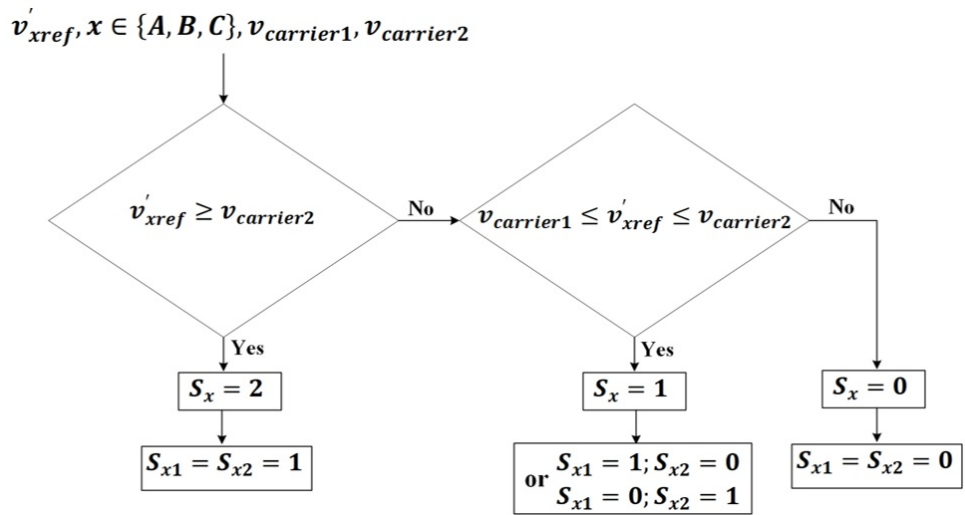


Figure 8: An algorithm for firing signals in IPD-SPWM and POD-SPWM.

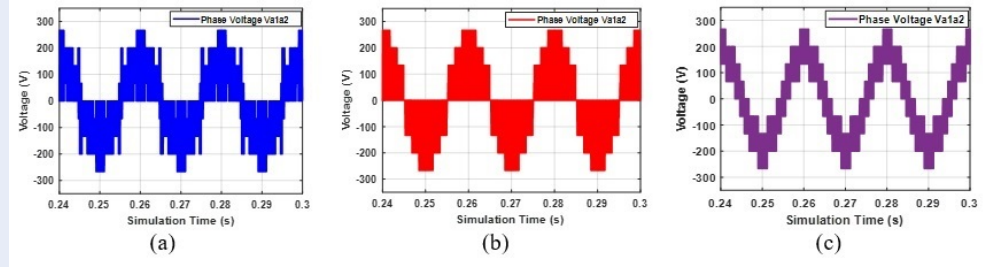


Figure 9: Phase-voltage waveforms of the **DTC-OEW** with isolated DC sources for  $m = 0.8$  under (a) RCMV1 (b) POD-SPWM and (c) IPD-SPWM.

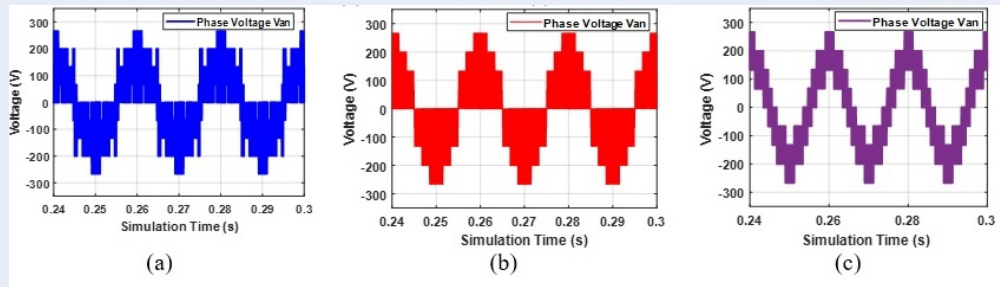


Figure 10: Phase-voltage waveforms of the **3L-NPC** for  $m = 0.8$  under (a) RCMV1 (b) POD-SPWM and (c) IPD-SPWM.

THD values. In particular, the THD value of phase voltage in the DTC-OEW is 47.87% in comparison to 47.9% in the 3L-NPC. For other modulation indices ( $m$ ), the THD of phase voltage with respect to  $m$  are shown in Figure 13(a) and (b) for the DTC-OEW and the 3L-NPC respectively. As can be seen in Figure 13, the THD curves of phase voltage are similar for both topologies under three PWM schemes. For instance, at  $m = 0.4$ , the THD values of phase voltage under RCMV1, POD-SPWM, and IPD-SPWM are 103.06%, 121.78%, and 74.96% respectively in the DTC-OEW as opposed to 103.2%, 121.96%, and 74.98% respectively in the 3L-NPC.

Regarding the THD of phase voltage under three PWMs schemes, IPD-SPWM consistently produces the lowest THD of phase voltage among the three, as shown in Figure 13, due to the use of three nearest voltage vectors. However, the CMV magnitude given by IPD-SPWM is twice as high as that of POD-SPWM and RCMV1 as illustrated in Figure 14(c) and Figure 15(c) for the DTC-OEW and the 3L-NPC. Meanwhile, POD-SPWM produces the highest THD of phase voltage among the three, as shown in Figure 13 while achieving reduced CMV magnitude, as indicated in Figure 14(b) and 15(b). In addition, under the condition of reduced CMV, as shown in Fig-

ure 14(a) and Figure 15(a), RCMV1 offers better output harmonic distortion than that of POD-SPWM, as indicated in Figure 13 (a) and (b) for the DTC-OEW and the 3L-NPC respectively. The frequency spectra of phase voltage in Figure 11 and 12 for the DTC-OEW and the 3L-NPC also confirms this. In which, the carrier-frequency components of phase voltage under RCMV1, POD-SPWM, and IPD-SPWM are 19%, 25%, and 11% respectively for both topologies. As for the CMV, the waveforms given by three PWM schemes for  $m = 0.8$  are shown in Figure 14 and Figure 15 for the DTC-OEW and the 3L-NPC respectively, indicating the resemblance between the two mentioned topologies. As shown in Figure 14 and Figure 15, IPD-SPWM produces the highest CMV magnitude of  $\frac{2V_{DC}}{3}$  as opposed to  $\frac{V_{DC}}{3}$  in RCMV1 and POD-SPWM. This fact is confirmed by the frequency spectra of CMV, as shown in Figure 16 and Figure 17 for the DTC-OEW and the 3L-NPC respectively. In particular, the carrier-frequency components of CMV under RCMV1 and POD-SPWM are about 20% as opposed to 40% under IPD-SPWM for both the DTC-OEW and the 3L-NPC.

Similar to the phase voltage, the same remarks can be made for the phase current. The phase current waveforms under three PWM schemes for  $m = 0.8$

are shown in Figure 18 and Figure 19 for the DTC-OEW and the 3L-NPC. The resemblance in these phase current waveforms is substantiated by the frequency spectra, as shown in Figure 20 and Figure 21 for the DTC-OEW and the 3L-NPC. Specifically, under RCMV1 and  $m = 0.8$ , the carrier-frequency component of phase current is 0.47% in the DTC-OEW in Figure 20 in comparison to 0.478% in the 3L-NPC in Figure 21.

With regard to the THD phase current under three PWM schemes, IPD-SPWM consistently yields the lowest THD values of phase current, as shown in Figure 22 for two topologies while producing the highest CMV magnitude of  $\frac{2V_{dc}}{3}$ . On the other hand, POD-SPWM gives the highest THD values of phase current while generating the reduced CMV magnitude of  $\frac{V_{dc}}{3}$ . Moreover, under the condition of reduced CMV, RCMV1 offers lower THD values of phase current than that of POD-SPWM, as evidenced in Figure 22 for both topologies. The frequency spectra of phase current in Figure 20 and Figure 21 at  $m = 0.8$  confirms the harmonic distortion of three PWM schemes. Specifically, the carrier-frequency components of phase current under RCMV1, POD-SPWM, and IPD-SPWM are around 0.47%, 0.65%, and 0.29% respectively for both topologies.

## CONCLUSION

The article has proposed the multilevel switching voltage models (ML-SVMs) for the DTC-OEW with isolated DC sources, which is equivalent to those of the 3L-NPC and the 3L-CHB, thereby enabling the DTC-OEW with isolated DC sources, the 3L-NPC, and the 3L-CHB to be regarded as a single multilevel-converter entity. Hence, this allows simple and intuitive PWM strategies previously applied to the 3L-NPC and the 3L-CHB to be directly utilized for the DTC-OEW with isolated DC sources without modification. With the help of the ML-SVMs, three PWM strategies, i.e., RCMV1, POD-SPWM, and IPD-SPWM, which are previously applied to the 3L-NPC are utilized for the DTC-OEW with isolated DC sources with detailed implementation, thus demonstrating the contribution of the ML-SVMs of the DTC-OEW. Simulation results obtained by these PWM schemes, including the waveforms of phase voltage, phase current, and CMV as well as their THD analyses and frequency spectra, are presented for the DTC-OEW and the 3L-NPC, indicating the equivalence of both ML-SVMs.

## LIST OF ABBREVIATIONS

DTC-OEW: Dual Two-level Converters with Open-end Winding Configuration

3L-NPCs: Three-level Neutral Point Clamped Converters

3L-CHBs: Three-level Cascaded H-bridge Converters

ML-SVMs: Multilevel Switching Voltage Models

SVM: Switching Voltage Model

IPD-SPWM: In-Phase Disposition Sinusoidal Pulse-width Modulation

POD-SPWM: Phase Opposition Disposition Sinusoidal Pulse-width Modulation

CMV: Common-mode Voltage

ZSV: Zero-Sequence Voltage

RCMV1: Reduced CMV Pulse-width Modulation

PWM: Pulse-width Modulation

## COMPETING INTERESTS

The authors declare that they have no competing interests.

## AUTHORS' CONTRIBUTIONS

Formal Analysis by Nho-Van Nguyen, Investigation by Khoa Dang Pham, Software by Khoa Dang Pham, Supervision by Nho-Van Nguyen, Validation by Nho-Van Nguyen, Writing – Original Draft by Khoa Dang Pham, Writing – Reviewing & Editing by Nho-Van Nguyen.

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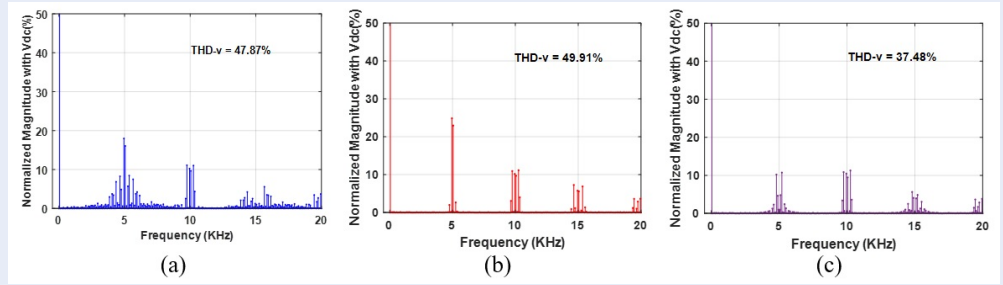


Figure 11: Frequency spectra of the Phase voltage waveforms in the **DTC-OEW** with isolated DC sources for  $m = 0.8$  under (a) RCMV1 (b) POD-SPWM (c) IPD-SPWM.

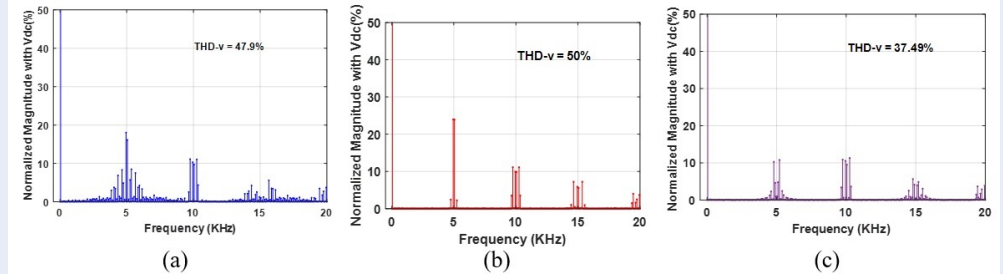


Figure 12: Frequency spectra of the Phase voltage waveforms in the **3L-NPC** for  $m = 0.8$  under (a) RCMV1 (b) POD-SPWM (c) IPD-SPWM.

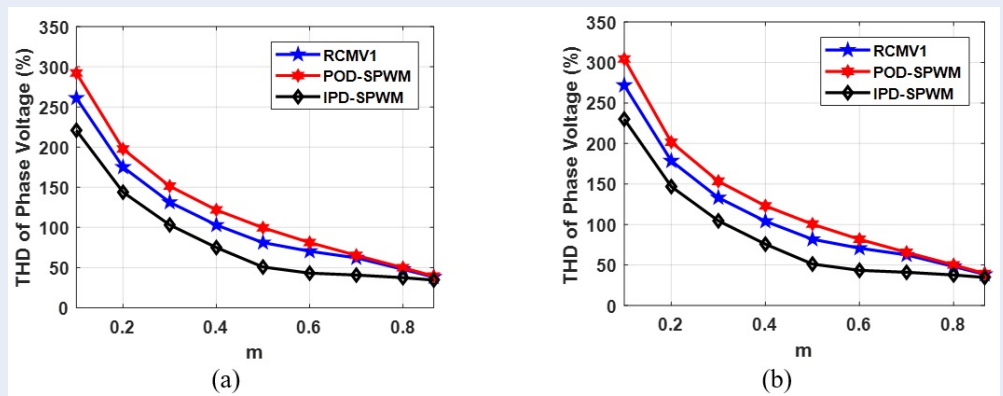


Figure 13: A comparative analysis of THD of phase voltage for (a) the **DTC-OEW** with isolated DC sources (b) the **3L-NPC** for RCMV1, IPD-SPWM, POD-SPWM.

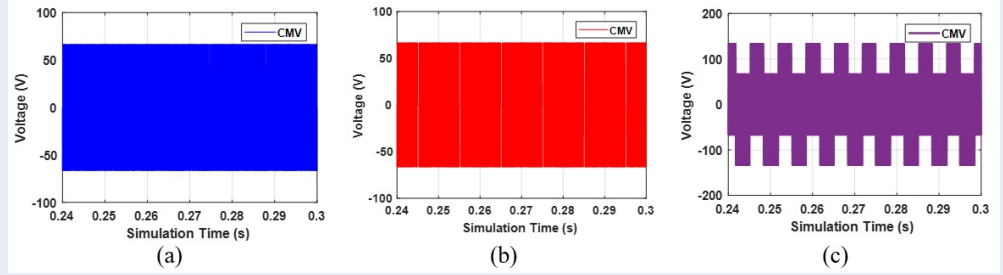


Figure 14: CMV waveforms of the **DTC-OEW** with isolated DC sources for  $m = 0.8$  under (a) RCMV1 (b) POD-SPWM and (c) IPD-SPWM.

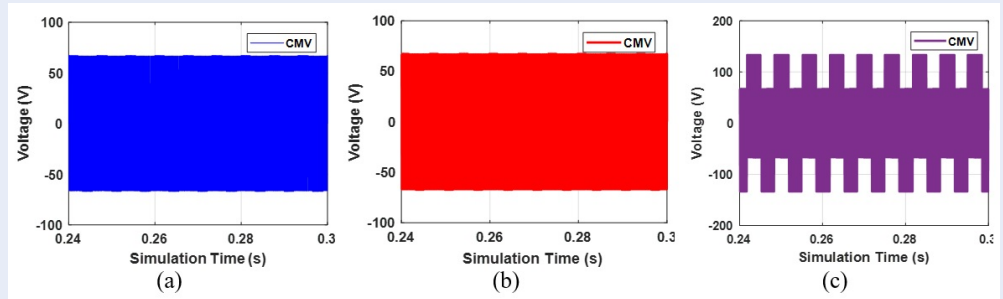


Figure 15: CMV waveforms of the **3L-NPC** for  $m = 0.8$  under (a) RCMV1 (b) POD-SPWM and (c) IPD-SPWM.

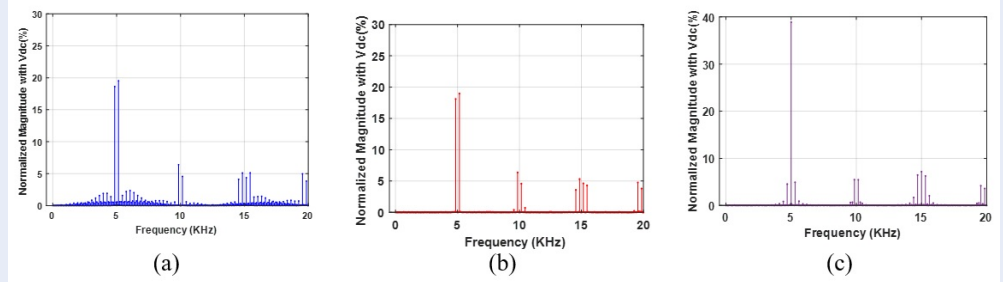


Figure 16: Frequency spectra of the CMV waveforms in the **DTC-OEW** with isolated DC sources for  $m = 0.8$  under (a) RCMV1 (b) POD-SPWM (c) IPD-SPWM.

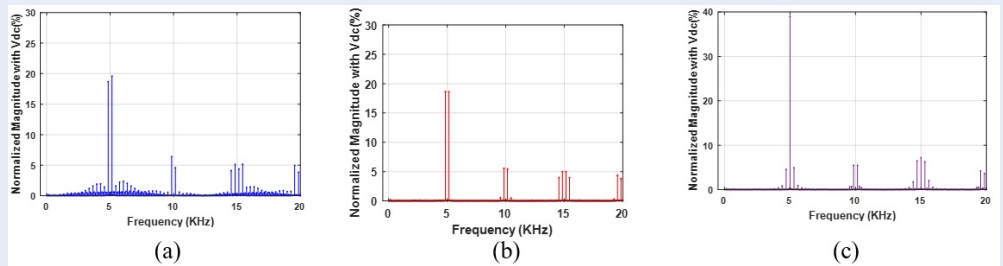


Figure 17: Frequency spectra of the CMV waveforms in the **3L-NPC** for  $m = 0.8$  under (a) RCMV1 (b) POD-SPWM (c) IPD-SPWM

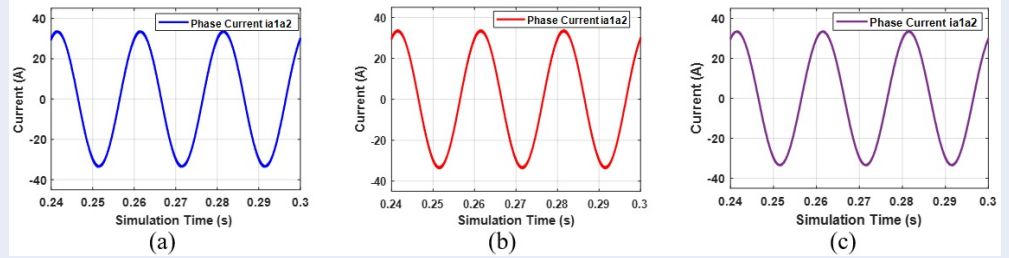


Figure 18: Phase-current waveforms of the **DTC-OEW** with isolated DC sources for  $m = 0.8$  under (a) RCMV1 (b) POD-SPWM and (c) IPD-SPWM.

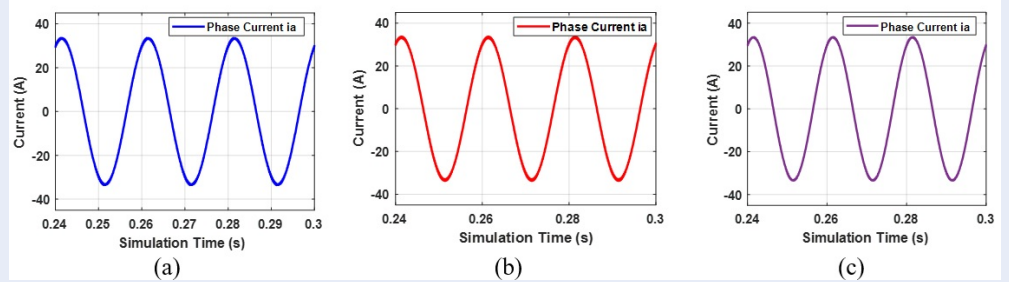


Figure 19: Phase-current waveforms of the **3L-NPC** for  $m = 0.8$  under (a) RCMV1 (b) POD-SPWM and (c) IPD-SPWM.

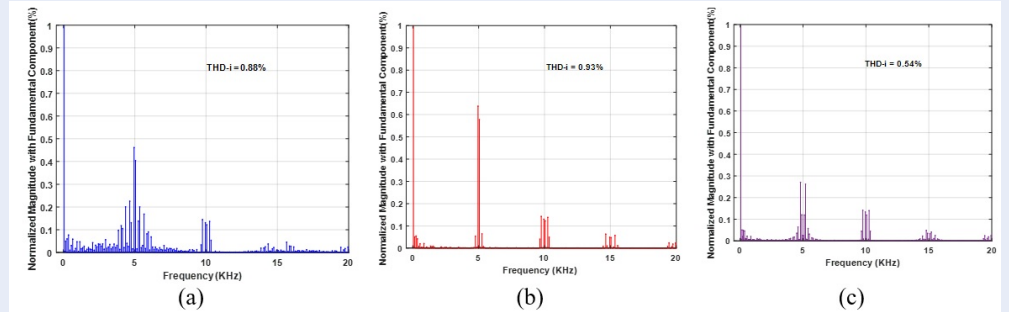


Figure 20: Frequency spectra of the Phase current waveforms in the **DTC-OEW** with isolated DC sources for  $m = 0.8$  under (a) RCMV1 (b) POD-SPWM (c) IPD-SPWM.

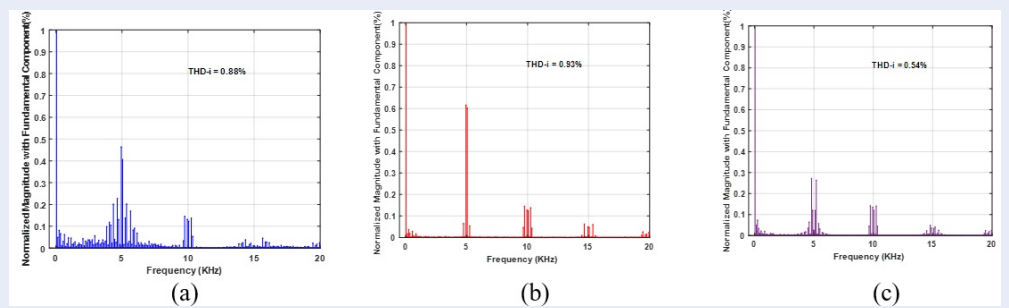
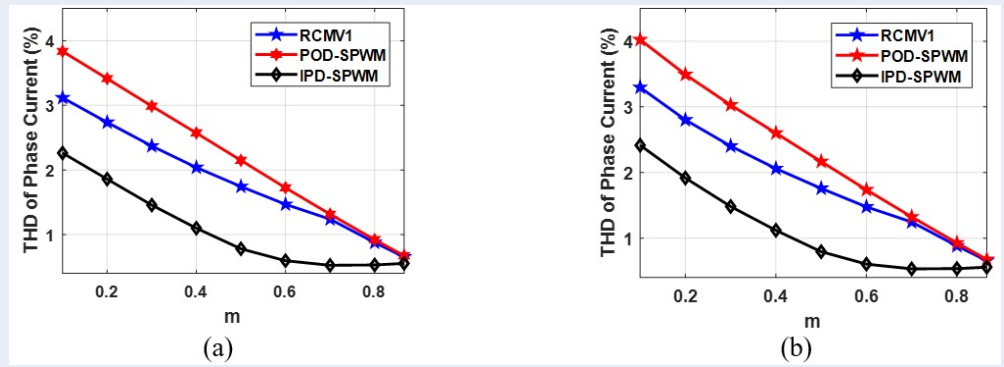


Figure 21: Frequency spectra of the Phase current waveforms in the **3L-NPC** for  $m = 0.8$  under (a) RCMV1 (b) POD-SPWM (c) IPD-SPWM.



**Figure 22:** A comparative analysis of THD of phase current for (a) the **DTC-OEW** with isolated DC sources (b) the **3L-NPC** for RCMV1, IPD-SPWM, POD-SPWM.

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# Mô hình hoá điện áp đóng ngắt và các phương pháp điều khiển độ rộng xung cho cấu hình hai bộ biến đổi hai bậc hở hai đầu

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## TÓM TẮT

Cấu hình hai bộ biến đổi hai bậc hở hai đầu (DTC-OEWs) mang nhiều tính năng ưu việt so với cấu hình ba bậc diode kẹp (3L-NPCs) như phân bố tổn hao đều trên các linh kiện, không yêu cầu cần bằng nguồn DC-link đầu vào và có nhiều trạng thái dư thừa. Tuy nhiên, các phương pháp điều khiển độ rộng xung (PWM) cho cấu hình hai bộ biến đổi hai bậc hở hai đầu phức tạp và không truyền thống. Do đó bài báo này trình bày mô hình áp đóng ngắt đa bậc cho cấu hình hai bộ biến đổi hai bậc hở hai đầu (OEW) dùng hai nguồn cách ly, bộ biến đổi ba bậc diode kẹp (3L-NPCs), và bộ biến đổi 3 bậc ghép tầng cầu H. Với mô hình áp đóng ngắt đa bậc, ba bộ biến đổi trên được coi như là một cấu hình. Do đó, với mô hình áp đóng ngắt đa bậc cho phép các phương pháp điều khiển độ rộng xung thực hiện đơn giản được áp dụng cho bộ biến đổi ba bậc diode kẹp và 3 bậc ghép tầng cầu H được áp dụng trực tiếp cho cấu hình hai bộ biến đổi hai bậc hở hai đầu. Một số phương pháp điều khiển độ rộng xung (PWM) được áp dụng cho bộ biến đổi ba bậc diode kẹp và ba bậc ghép tầng cầu H được áp dụng cho cấu hình hai bộ biến đổi hai bậc hở hai đầu bằng việc sử dụng mô hình áp đóng ngắt. Kết quả mô phỏng của các phương pháp điều khiển độ rộng xung cho ba cấu hình trên như dạng sóng điện áp dây, dòng pha, và điện áp Common-mode cho thấy sự giống nhau hoàn toàn. Do đó, điều này minh chứng sự đúng đắn của mô hình áp đóng ngắt đa bậc được đề xuất trong bài báo.

**Từ khoá:** cấu hình ghép tầng cầu H, mô hình hoá bộ biến đổi đa bậc, bộ biến đổi đa bậc diode kẹp, bộ biến đổi hở hai đầu, phương pháp điều khiển độ rộng xung

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